CLAIMS

I claim:

1. A method for performing design verification, the method comprising:

specifying at least one object that represents at least one signal as a symbol in a design using a first programming interface call (PLI) command; and

instructing a symbolic simulator with the first command to treat the at least one object as a symbol.

2. The method defined in Claim 1 further comprising:

inserting the first command into a design specification; and

inputting the design specification into the symbolic simulator.

3. The method defined in Claim 1 wherein the at least one object comprise a hardware description language object.

4. The method defined in Claim 1 wherein the at least one object comprises a Verilog object.

5. The method defined in Claim 1 wherein the first command comprises a Programming Language Interface (PLI).

6. The method defined in Claim 1 wherein the at least one signal comprises an input.

7. The method defined in Claim 1 further comprising:

specifying a check using a second command, the check to perform a test to validate design functionality; and

instructing the symbolic simulator using the second command to perform the test.

8. The method defined in Claim 7 further comprising:

inserting the first and second commands into a design specification; and

inputting the design specification into the symbolic simulator.

9. The method defined in Claim 7 wherein the second command comprises a PLI.

10. The method defined in Claim 7 further comprising:

instructing the symbolic simulator to generate a file with information to locate an identified fault.

11. An article of manufacture having at least one recordable medium having stored thereon executable instructions which, when

executed by at least one processing device, cause the at least one processing device to:

specify at least one object that represents at least one signal as a symbol in a design using a first command; and

instruct a symbolic simulator with the first command to treat the at least one object as a symbol.

12. The article of manufacture defined in Claim 11 further comprising executable instructions stored on the at least one recordable medium which, when executed by at least one processing device, cause the at least one processing device to:

insert the first command into a design specification; and

input the design specification into the symbolic simulator.

13. The article of manufacture defined in Claim 11 wherein the at least one object comprise a hardware description language object.

14. The article of manufacture defined in Claim 11 wherein the at least one object comprises a Verilog object.

15. The article of manufacture defined in Claim 11 wherein the first command comprises a Programming Language Interface (PLI).

16. The article of manufacture defined in Claim 11 wherein the at least one signal comprises an input.

17. The article of manufacture defined in Claim 11 further comprising executable instructions stored on the at least one recordable medium which, when executed by at least one processing device, cause the at least one processing device to:

specify a check using a second command, the check to perform a test to validate design functionality; and

instruct the symbolic simulator using the second command to perform the test.

18. The article of manufacture defined in Claim 17 further comprising executable instructions stored on the at least one recordable medium which, when executed by at least one processing device, cause the at least one processing device to:

insert the first and second commands into a design specification; and

input the design specification into the symbolic simulator.

19. The article of manufacture defined in Claim 17 wherein the second command comprises a PLI.

20. The article of manufacture defined in Claim 17 further comprising executable instructions stored on the at least one recordable medium which, when executed by at least one processing device, cause the at least one processing device to:

instruct the symbolic simulator to generate a file with information to locate an identified fault.